A prototype scalable readout system for micro-pattern gas detectors*

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Abstract: A scalable readout system (SRS) is designed to provide a general solution for different micro-pattern gas detectors in various applications. The system mainly consists of three kinds of modules: the ASIC card, the adapter card and the front-end card (FEC). The ASIC cards, mounted with particular ASIC chips, are designed for receiving detector signals. The adapter card is in charge of digitizing the output signals from several ASIC cards. The FEC, edged-mounted with the adapter, has field-programmable gate array (FPGA)-based reconfigurable logic and I/O interfaces, allowing users to choose different ASIC cards and adapters for different experiments, which expands the system to various applications. The FEC transfers data through Gigabit Ethernet protocol realized by a TCP processor (SiTCP) IP core in FPGA. By assembling a flexible number of FECs in parallel through Gigabit Ethernet, the readout system can be tailored to specific sizes to adapt to the experiment scales and readout requirements. In this paper, two kinds of multi-channel ASIC chip, VA140 and AGET, are applied to verify the scalability of this SRS architecture. Based on this VA140 or AGET SRS, one FEC covers 8 ASIC (VA140) cards handling 512 detector channels, or 4 ASIC (AGET) cards handling 256 detector channels, respectively. More FECs can be assembled in crates to handle thousands of detector channels.

Keywords: scalable readout system (SRS), micro-pattern gas detectors (MPGD), charge measurement, front-end electronics, VA140, AGET

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1 Introduction

As fundamental components of high energy physics (HEP) experiments, micro-pattern gas detectors (MPGDs) offer great potential as high resolution particle tracking detectors for a variety of applications, especially the Micromegas [1] and Gas Electron Multipliers (GEMs) [2], which have now reached maturity and become increasingly important. MPGDs have already been used in large-scale particle physics experiments, like COMPASS [3, 4], ALICE [5] and LHCb [6]. They are used as the forward detectors [7–11] thanks to characteristics such as excellent time and spatial resolution, high radiation resistance, high rate capability, and large active areas.

The widespread uses of the MPGD are a driving factor in the development of corresponding readout electronics. Various applications call for a variety of appropriate readout requirements (signal polarity, radiation tolerance, a certain number of channels, etc.), which urges scientists to establish a scalable multichannel readout system. Therefore, in 2009, the RD51 Collaboration at CERN [12] produced the most promising readout electronics system, named the Scalable Readout System (SRS), for gas detectors like Micromegas and GEMs, featuring a scalable architecture and a general-purpose chip link interface, allowing the user to choose from a variety of front-end chips on hybrids with integrated spark protection circuitry [13]. Since the first SRS systems were successfully used in ATLAS Micromegas stations in 2010, the readout system progressively gained momentum in the MPGD community. At present, the SRS system has already been considered to be established as an industry standard abroad [13], but in China there has been little study of this area. This paper presents a prototype SRS system designed by the authors' group.

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2 Proposed architecture

Referencing the design concept presented by the RD51 collaboration, the architecture of the authors' prototype SRS is shown in Fig. 1. The readout electronics mainly consist of three kinds of modules, the analog module called the ASIC card, which is the nearest part to the detector and measures charge signals, the analog to digital module named the adapter card, sampling the analog module outputs, and the digital module named the front-end card (FEC), which is responsible for signal processing and transmitting and receiving of data and control commands. Using a "Several-in-One" strategy, several particular ASIC cards are connected to one specific designed adapter through a general purpose chip link, and the adapter is edged-mounted to the fixed FEC through SAMTEC PCIe connectors as a standard 6U*220 mm plug-in. An AC/DC power module energizes the three kinds of cards. All of the plug-ins and power module are assembled in a 6U crate. After processing the digitized data, the FEC transmits data to and from the server or PC.

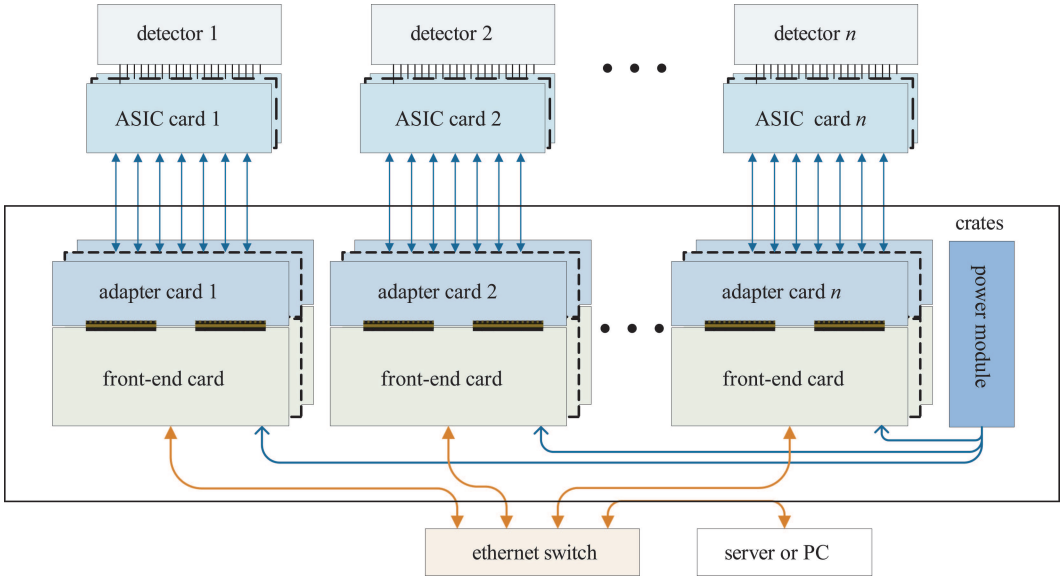

Fig. 1. (color online) Block diagram of the proposed SRS.

As shown in Fig. 1, based on different multi-channel ASIC chips, n types of ASIC cards with corresponding Adapters are designed for different experiments because in a certain target experiment, usually only one kind of ASIC chip is the best fit. The FEC contains FPGA-based reconfigurable control-logic and I/O interfaces for different specific adapters. Through reconfiguring, all kinds of ASIC cards and adapters can work normally under the control of the FEC with fixed hardware. Therefore, just by changing some of the system cards, the flexible SRS architecture fits the various requirements of MPGD which is widely used in many fields.

In the "Several-in-One" strategy, several ASIC cards are controlled by one FEC. So, one FEC can handle a certain number of detector channels which is determined by the particular multi-channel ASIC chip. For a small system, one FEC is sufficient to meet the quantity requirement of detector channels. Furthermore, using Gigabit Ethernet for FEC connections, forming a larger system of more FECs for large scale experiments is flexible. A number of FECs could be assembled in parallel to expand the number of detector channels which are read out.

3 Implementation of the SRS

The prototype SRS system is designed and verified with two multi-channel ASIC chips, VA140 [14] and AGET [15], which are suitable for MPGDs. Photographs of the system are shown in Fig. 2. Two sets of ASIC cards with corresponding Adapters are specially designed. The fixed FEC matches the Adapters and forms a standard 6U*220 mm Eurocard which would be assembled in a crate.

3.1 The crate

As shown in Fig. 2, a standard 19-inch crate, designed and custom made from SCHROFF with 19 slots

at most, is used to assemble the 6U*220 mm plug-ins. Mounted at the rear of the crate, the stabilized power module (13100-145, SCHROFF) [16] with input voltage ranging from 90 to 264 $V_{AC,}$ supplies 4 high current output powers ($+3.3V_{DC}$(60 A), $+5.0V_{DC}$(50 A), $+12V_{DC}$(12 A), $-12V_{DC}$(12 A)) for the SRS system.

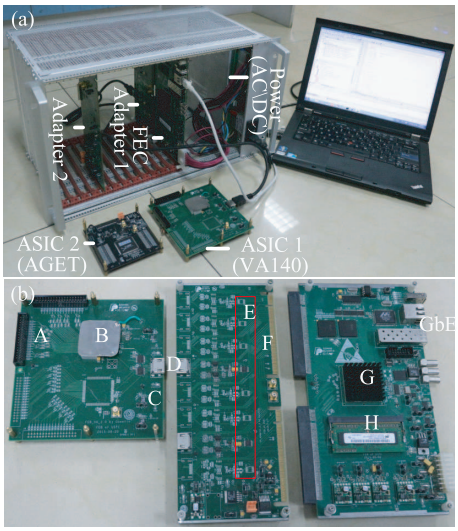

Fig. 2. (color online) (a) A photograph of the SRS crate and its prototype modules. (b) Cards based on VA140: A — ESD diodes; B — VA140; C — LDO; D — HDMI connector; E — 8 ADCs; F — PCIe finger connector; G — Virtex 6 FPGA; H — DDR3.

3.2 The FEC card

The FEC module is designed around a Virtex 6 FPGA (XC6VLX240T) as a 6U*120 mm card, integrating one DDR3 memory chip, one Ethernet port and general interfaces, as shown in Fig. 3. At the front end, the detector signals are integrated, shaped by the ASIC cards and then amplified, sampled by the adapter, under the control of the FPGA. The FPGA receives the digitized data through SAMTEC PCIe connectors for further processing. In FPGA, data selection algorithms must be developed to meet the requirements of different experiment. The target data is formatted and stored in the DDR3 buffer. For data transmission, we study the SiTCP [17], which is a hardware-based TCP processor for devices limited by hardware size, such as front-end devices or detectors. The SiTCP processes TCP, IP and Ethernet protocols to realize the process of data transmission. A Gigabit-Ethernet media independent interface (GMII) is used to link the Ethernet physical layer device (PHY) and a media access controller (MAC). The details of the same data transmission based on SiTCP are described in Ref. [18].

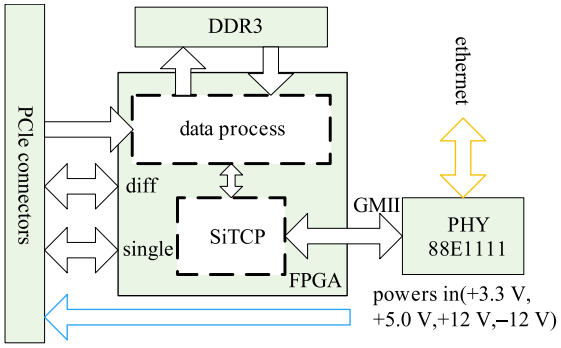

Fig. 3. Block diagram of FEC.

To serve the needs of scalability, the redundancy is fully considered in designing a FEC which may cover potential ASIC cards based on different multi-channel chips. Two PCIeX16 connectors are chosen. Both the differential and single IOs of the FPGA are routed to this PCIe interface, with plenty of design redundancy including sufficient IOs, same length of wires (25 mils margin for differential wires, and 50 mils margin for single wires), etc., as shown in Table 1. Figure 4 shows part of the PCIe connections. Four kinds of power supplies from the AC-DC power module are also connected to the PCIe connector. Through reconfiguring the interface, specific adapters and corresponding ASIC cards work normally under the control of the FEC. By choosing different adapters and corresponding ASIC cards for different target experiments, the SRS architecture expands the system to various applications. Furthermore, a number of FECs can be assembled in a topology through the Gigabit Ethernet port. This method makes the SRS suitable for experiments with large number of detector channels.

Table 1. Redundancy design list of PCIe connectors on FEC.

types	numbers	connected
powers	4 kinds	AC/DC module
single	74 wires	FPGA
differential	34 pairs	FPGA
clock	1 pair	system clock

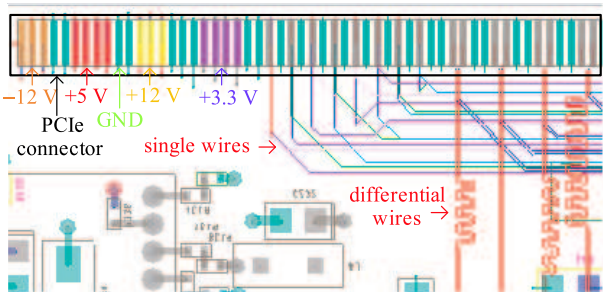

Fig. 4. (color online) Part of FEC PCB layout for PCIe connections.

3.3 Specific ASIC cards and adapters

Many potential multi-channel ASIC chips such as VA140 [14], AGET [15] and APV25 [19] etc. , are suitable for MPGDs in various applications. In this section, the design structure and proposal for ASIC cards and adapters are presented first, as shown in Figs. 5 and 6. Then, 2 kinds of ASIC cards and adapters are implemented based on VA140 and AGET to verify the concept of this SRS architecture.

The ASIC card is installed close to the detector and shielded by the metal structure, which greatly reduces the noise and avoids interference from external electromagnetic fields. As shown in Fig. 5, the input channels of ASIC chips are AC coupled ($C = 10$ nF) to the detectors and protected against electrostatic discharge (ESD) by diode arrays (NUP4114UPXV6) tested with a level 4 contact discharge of 8 kV according to the IEC 61000-4-2 standard [20]. When the MPGD charge signal, with a pulse width from tens of ns to about 100 ns [1, 2], is applied to the 10 nF AC coupled capacitor, the equivalent impedance of about 1 ohm is much less than the output impedance of the detector and can be ignored.

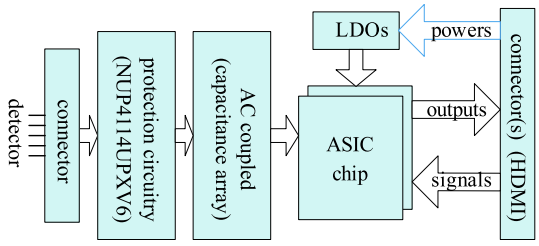

Fig. 5. Block diagram of ASIC card.

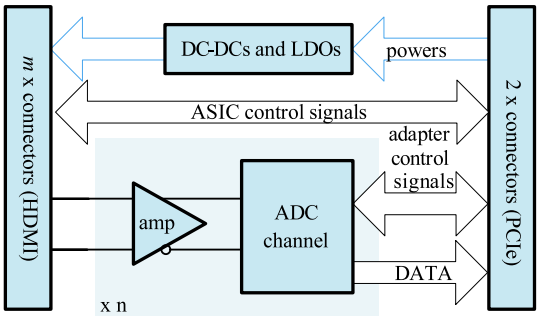

Fig. 6. Block diagram of adapter card.

The HDMI type-A-to-type-A cable is shown in Fig. 7 is adopted for this system. It features four high-speed 100 ohms differential pairs for critical signals, 7 single pins for common signals, and 500 mA per pin for power supplies. The shielded differential pairs are used for transferring ASIC chip outputs to avoid crosstalk. Since the ASIC cards need particular power supplies which are regulated by the local LDOs, the initial voltages are supplied via the HDMI cable from the adapter, in the same way that the ASIC control signals and ASIC outputs are transferred between the two cards.

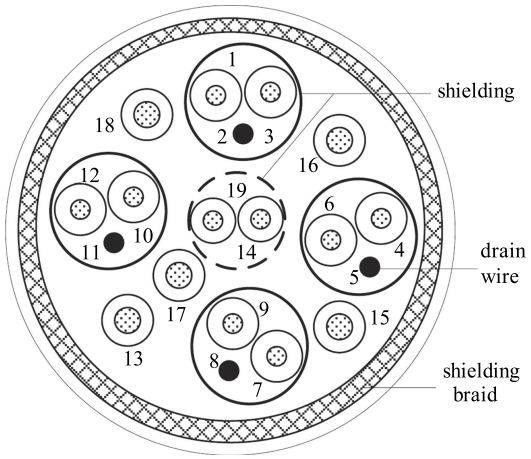

Fig. 7. Cross-section of HDMI type-A-to-type-A cable.

The adapter is a link between the ASIC cards and FEC. As shown in Fig. 6, it is designed based on ADCs and tailored to fit the FEC through PCIe connectors. The ASIC and adapter control signals are produced by the FPGA on the FEC, which also supplies power to them. The particular power supplies needed for the adapters are regulated by local DC-DC converters and LDOs.

3.3.1 ASIC cards and adapter based on VA140

Following the design structure and proposal described earlier, the first set of ASIC card and corresponding adapter were designed based on a VA140 chip [14] which is a 64-channel, 6.5 μs peaking time, low-noise, low power, and high dynamic range (from −200 fC to 0 or from 0 to 200 fC) charge sensitive preamplifier-shaper ASIC, suitable for MPGDs and silicon detectors [18]. An overview and partial performance of the chip are described in Ref. [21].

Table 2. Definition of the HDMI cable for controlling the VA140 based ASIC card.

pin number	definition	pin number	definition
2	GND	11	GND
3	DRESET	12	TEST_ON
1	SHIFT_IN_B	10	CLKB
5	GND	17	GND
6	VA2_OUT_P	19	+3.3V
4	VA2_OUT_N	14	−3.3V
8	GND	13	−3.3V
9	VA1_OUT_P	15	HOLDB
7	VA1_OUT_N	16	GND
		18	+3.3V

Table 3. Power supplies of adapter and power consumptions of ASIC card based on VA140.

adapter card	power supplies	ASIC card	power consumptions
3.3 V	TPS74401 (3 A)	3.3 V	<25 mA
−3.3 V	PTN04050A1 (1 A)	−3.3 V	<18 mA
−3.3 V	PTN04050A2 (1 A)		

According to the VA140 datasheet [14], the chip needs 1.5 V and −2.0 V power supplies, 5 single controlling signals (HOLDB, CLKB, SHIFT_IN_B, DRESET, and TEST_ON), and 1 differential output. The power consumption of the VA140 is about 0.29 mW/ch and the noise is about 0.068 fC ($C_{\rm in}$=50 pF). The LDO regulators (LT3605 and LT3090) on the ASIC card are used for 3.3 V to 1.5 V converting and −3.3 V to −2.0 V converting, respectively. The initial 3.3 V and −3.3 V power levels, which are regulated by LDO (TPS74401) from 5.0 V to 3.3 V (3 A) and DC-DC converters (2 PTN04050A,) from 5.0 V to −3.3 V (2 A) on the Adapter, respectively, are supplied via the HDMI cable. The definition of the HDMI cable is shown in Table 2. In the VA140 based SRS, one ASIC card integrates 2 VA140 chips. Each VA140 channel integrates its eventual signal for 6.5 μs. After the peak is reached (6.5 μs), an external 'HOLDB' signal should be applied to sample the value. Immediately after this, a sequential read-out can be performed by activating the output bit-register using 'SHIFT_IN_B' and 'CLKB'. Only one channel at a time can be seen on the output of the chip. The 64 channel outputs of VA140 are read out in sequence from the top to the bottom channel by clocking 'CLKB' (usually from several KHz to several MHz). In order to sample all the channel values, a 12-bit dual-ADC chip (AD7356) is adopted to digitalize the output of VA140, with a good performance from 0 to 5 MSPS which covers the clocking 'CLKB' range. For this VA140-based SRS, charge measurement from 0 to -200 fC with an accuracy of better than 1 fC is supposed. So the quantization error of the 12 bit ADC, which is 0.025% (0.05 fC), can be ignored. The ADC just needs 4 controlling signals (SCLK, SDATA_A, SDATA_B, and CS) to work normally, which helps the scalability of the system. With some other auxiliary devices, the VA140 ASIC card and Adapter are implemented. The power supplies from Adapter to ASIC card via HDMI cable are shown in Table 3. It should be pointed out that the VA140 chip in this project is encapsulated in the CQFP132 package. Limited by the packaging technology, only 32 channels per chip are wire bonded out.

In the VA140 based SRS, the FEC with corresponding adapter is responsible for digitization of the front-end signals and acts as a carrier for the "8-in-1" card. Eight VA140 ASIC cards read out 512 detector channels and connect to one adapter which integrates 8 ADC chips (AD7356).

3.3.2 ASIC cards and adapter based on AGET

The second set of ASIC card and corresponding adapter is designed based on an AGET chip [15], which is specifically developed for Generic Electronics systems for Time Projection Chambers (GET) [22, 23]. The chip includes 64 channels and every channel consists of a charge sensitive preamplifier (CSA), a shaper, a discriminator and a 512-sample analog memory. The chip can be programmed to work in various modes with different charge ranges (120 fC, 240 fC, 1 pC and 10 pC), peaking time (16 values from 50 ns to 1 μs), sampling frequency (1 MHz to 100 MHz), and signal polarity (positive or negative). These characteristics give it a wide variety of roles in high energy physics experiments.

Table 4. Definition of the first HDMI cable for controlling the AGET-based ASIC card.

pin number	definition	pin number	definition
2	GND	11	GND
3	AGET_OUT_P	12	RCKP
1	AGET_OUT_N	10	RCKM
5	GND	17	GND
6	TRIGGP	19	GND
4	TRIGGM	14	WRITE
8	GND	13	GND
9	WCKP	15	GND
7	WCKM	16	READ
		18	GND

Table 5. Definition of the second HDMI cable for controlling the AGET-based ASIC card.

pin number	definition	pin number	definition
2	GND	11	GND
3	SC_DOUT	12	SC_DIN
1	GND	10	GND
5	GND	17	GND
6	SC_CK	19	+5V
4	GND	14	+5V
8	GND	13	GND
9	SC_EN	15	GND
7	GND	16	+5V
		18	GND

Table 6. Power supplies of adapter and power consumptions of ASIC card based on AGET.

adapter card	power supplies	ASIC card	power consumptions
5.0V	AC/DC module	5.0 V	$\sim$300 mA

According to the AGET datasheet [15], the chip counting rate is less than 1 kHz. The chip needs a 3.3 V power supply, 3 pairs of differential controlling signals (TRIGGP, TRIGGM, WCKP, WCKM, RCKP, RCKM), 6 single controlling signals (WRITE, READ, SC_DOUT, SC_DIN, SC_CK, SC_EN), and 1 differential output. The power consumption of the AGET chip is about 10 mW/ch. The LDO regulator (LT1963A) on the ASIC card converts the voltage from 5.0 V to 3.3 V, and the initial 5.0 V is supplied via the HDMI cable from the adapter. The AGET-based ASIC card includes 2 HDMI connectors and the definition of the 2 HDMI cables is shown in Tables 4 and 5. In the AGET-based SRS, 4 AGET ASIC cards connecting to 1 adapter are designed. Each ASIC card integrates 1 AGET chip. The input signal of each AGET channel is filtered, amplified and sampled in the 512-sample analog memory. In the readout phase, the analog data from the different channels is multiplexed toward a single output at the readout frequency of 25 MHz. To digitalize the outputs of AGET chips, a 14-bit quad-ADC (AD9259) is adopted to connect to 4 AGET chips, featuring up to 50 MSPS, which samples 1 or 2 points of the AGET output. For the AGET chip, the noise is about 0.14 fC ($C_{\rm in}$=30 pF, 120 fC) [15]. So the quantization error of the 14 bit ADC, which is 0.007% (0.008 fC), can be ignored. The ADC works normally with 7 pairs of differential controlling signals (ADC_CLKP, ADC_CLKN, DCO_P, DCO_N, FCO_P, FCO_N, 4 pairs of ADC output signals), and 4 single control signals (CSB, SDIO, SCLK, POWN). With the help of some other auxiliary devices, the AGET ASIC card and adapter are implemented.

In the AGET-based SRS, the FEC with corresponding Adapter acts as a carrier for the "4-in-1" card. Four AGET ASIC cards read out 256 detector channels and are connected to one adapter.

4 Test results

The prototype SRS with two sets of ASIC cards and adapters based on VA140 and AGET were implemented and assembled respectively. In this section, the performance of the VA140 and AGET chips is tested first, then the transfer performance of the FEC based on SiTCP, and the power consumption.

Due to the VA140 and AGET chips both having calibration capacitors on chip, a general testing method was used: a waveform generator (Tektronix, AFG3252) with attenuator was used to generate step pulses with different amplitudes. When the step pulses were applied to the on-chip capacitor, a certain amount of charge, which covered the full range, was injected into the selected channel of the VA140 or AGET for performance testing.

In the VA140-based SRS, step pulses with amplitude ranging from 2 to 120 mV and 100 ns trailing edge were applied to the on-chip capacitor (2 pF), and a certain amount of charge, from 4 fC to 240 fC, which covered the full range, was injected into the 32 channels of the VA140 respectively. A typical relationship between output peak value and input charge of the system is shown in Fig. 8 (a). The quadratic curve indicates that the integral nonlinearity (INL) was better than 1.5%. The noise (RMS) was about 0.15 fC without connecting to the detector.

In the AGET-based SRS, the chip had a large number of operation modes. The charge measurement was tested with the 120 fC range. The step pulses with amplitude ranging from 100 to 1000 mV and 100 ns trailing edge were applied to the on-chip capacitor (120 fF), and a certain amount of charge, from 12 fC to 120 fC, which covered the full range, was injected into the selected channel of the AGET. A typical linearity curve of output peak value versus input charge is shown in Fig. 8 (b), with an INL of better than 2%. The noise was better than 0.2 fC without connecting to the detector.

In order to test the transfer performance of FEC, the FEC was connected directly to a PC with a standard RJ-45 cable, acting as a TCP server and TCP client, respectively. The transfer speed can reach up to 530 Mbps per FEC. The power consumption of the FEC was about 10 W (3.3 V (2.8 A), 5.0 V (0.16 A)).

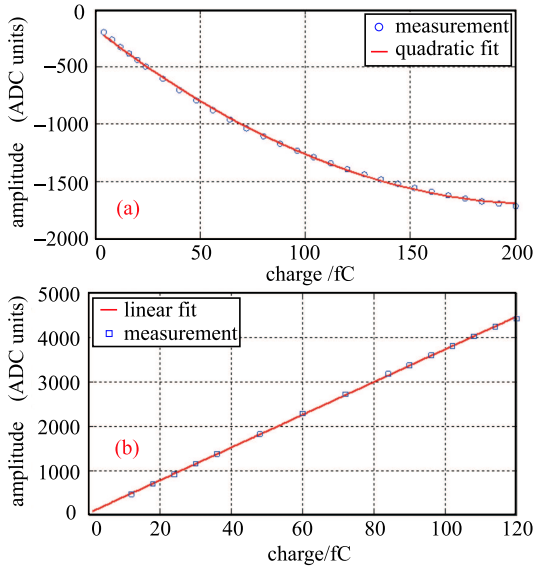

Fig. 8. (color online) (a) The quadratic fit result of VA140 with an INL of better than 1.5%. (b) The linear fit result of AGET with an INL of better than 2%.

5 Conclusion

A prototype SRS system, including three kinds of modules: the ASIC card, the adapter card and the FEC,

have been designed and tested with good performances. The fixed FEC offers a reconfigurable interface for potential ASIC chips, expanding the system in various applications. A standard 19-inch crate is designed to assemble the FECs, which can be tailored to specific sizes to adapt to the experiment scales.

Two sets of ASIC (VA140 and AGET) cards with corresponding adapters were specifically designed to verify the scalability of the SRS. The VA140-based SRS has a good INL (better than 1.5% from 0 to −200 fC) and low noise (about 0.15 fC); The AGET-based SRS has a good INL (better than 2% from 0 to −120 fC) and low noise (less than 0.2 fC). In the SRS, one FEC covers 8 ASIC (VA140) cards handling 512 detector channels, or 4 ASIC (AGET) cards handling 256 detector channels, respectively. Taking the VA140-based SRS as an example, one crate has an ability to assemble 17 FECs (another two slots for one power module), integrating 272 VA140 chips which handle 8704 detector channels. If all of the 64 channels of the VA140 are bonded out in our future work, one crate can handle 17408 detector channels. Such a readout system can be tailored for use in many future HEP experiments and other application fields, like medical imaging and industry with MPGDs.

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