Study of silicon pixel sensor for synchrotron radiation detection *

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Abstract: The silicon pixel sensor (SPS) is one of the key components of hybrid pixel single-photon-counting detectors for synchrotron radiation X-ray detection (SRD). In this paper, the design, fabrication, and characterization of SPSs for single beam X-ray photon detection is reported. The designed pixel sensor is a p+-in-n structure with guard-ring structures operated in full-depletion mode and is fabricated on 4-inch, N type, 320 μm thick, high-resistivity silicon wafers by a general Si planar process. To achieve high energy resolution of X-rays and obtain low dark current and high breakdown voltage as well as appropriate depletion voltage of the SPS, a series of technical optimizations of device structure and fabrication process are explored. With optimized device structure and fabrication process, excellent SPS characteristics with dark current of 2 nA/cm^2, full depletion voltage < 50 V and breakdown voltage > 150 V are achieved. The fabricated SPSs are wire bonded to ASIC circuits and tested for the performance of X-ray response to the 1W2B synchrotron beam line of the Beijing Synchrotron Radiation Facility. The measured S-curves for SRD demonstrate a high discrimination for different energy X-rays. The extracted energy resolution is high ($< 20\%$ for X-ray photon energy > 10 keV) and the linear properties between input photo energy and the equivalent generator amplitude are well established. It confirmed that the fabricated SPSs have a good energy linearity and high count rate with the optimized technologies. The technology is expected to have a promising application in the development of a large scale SRD system for the Beijing Advanced Photon Source.

Keywords: synchrotron X-ray, silicon pixel sensor, dark current, energy resolution, count rate

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1   Introduction

For current high-resolution and high-sensitivity synchrotron radiation detection (SRD), low dark current noise, short readout time in the millisecond range, and high dynamic range are generally required for a high performance SRD system. Complicated SRD systems of hybrid pixel single-photon-counting detectors have recently been successfully developed for SRD in the soft X-ray range [1, 2]. The hybrid pixel detector is composed of a pixel sensor and readout electronics as well as a bump-bonding package part, which is applied to bond these two components together. The pixel sensor, which detects the incident X-ray synchrotron radiation, is the main part of the system and is generally made by conventional semiconductor processes on semiconductor substrate. The silicon (Si) pixel sensor (SPS) made by the Si planar process is the most common type [3-6] and demonstrates an excellent performance and the best flex-ibility in system integration.

To achieve high resolution and high sensitive SRD for X-rays, low dark current and high breakdown voltage as well as appropriate depletion voltage of SPS is necessary for detection system integration. It involves a series of technical optimizations on device structure and fabrication process as well as testing and debugging of system integration [7–9]. In this paper, aiming to apply hybrid pixel detectors for SRD in BAPS (Beijing Advanced Photon Source), the device structure and fabrication process of SPS are investigated in detail. Some critical electrical parameters are optimized with special structure design and improved process technologies. The fabrication process is finished on the Si fab-line of the Institute of Microelectronics of the Chinese Academy of Sciences. The fabricated SPSs are successfully integrated with the fabricated ASIC read circuits using metal wire-bonding technology. The sensor's response to X-ray radiation has been tested and analyzed in detail. From the

ASIC S-curve, the sensor's energy resolution is excellent and the linear response between input X-ray energy and the equivalent generator amplitude are well established. The results confirm the validity of the design and optimizations of SPD technologies.

2   Si pixel sensors (SPS) structure and process

SPSs are a kind of special p$^+$-in-n (PIN) diode on high resistivity Si substrate fabricated with a conventional Si planar process. They need a special device structure designed to reduce the dark current and to avoid breakdown [6]. The fabrication processes, such as oxide thickness, implant dose and energy, junction thickness and integration flow, also need to be optimized to achieve excellent electrical characteristics. We have designed a series of various pixel layouts to optimize the device structure for the best performance. Pixels with different sizes, spaces and guard-rings are simulated or fabricated to evaluate their electrical results. The test structures on the fabricated wafer consist of several arrays of 8×8 SPS with guard rings on the device side and the other isolated devices for device or process monitoring. Pixel arrays were made on a 4-inch-diameter n-type < 111 > wafer with a thickness of 300 μm and resistivity of 6−8 kΩ·cm. The pixel size ranged from 180 μm to 150 μm with different device structures. The typical

parameters of the PIN pixel sensors are summarized in Table 1.

Table 1.   Typical parameters of PIN_Si pixel sensors.

parameter	value
silicon wafer	4 in. n-type
crystal	$< 111 >$
resistivity	7 kΩ·cm
thickness	300–320 μm
pixel size	180×180–150×150 μm^2
number of pixels	8×8=64 for test

The pixel sensor was designed to be a square PIN diode with five guard rings. Figure 1 shows a cross-sectional view of the device. The 8×8 pixels were used to test the critical electrical parameters of the dark current and the junction capacitance. Following the design route in the Si planar process, technology computer-aided design (TCAD) is adopted to optimize the sensor structure and verify the fabrication process. Though the TCAD is capable of 3D simulations of the whole pixel array, we use the TCAD to simulate the typical sensors in two dimensions, which can simplify the simulation process time and is sufficient to evaluate the device characteristics we explored. The process optimization items of the TCAD are: oxidation, deposition, etching, ion implantation, and annealing.
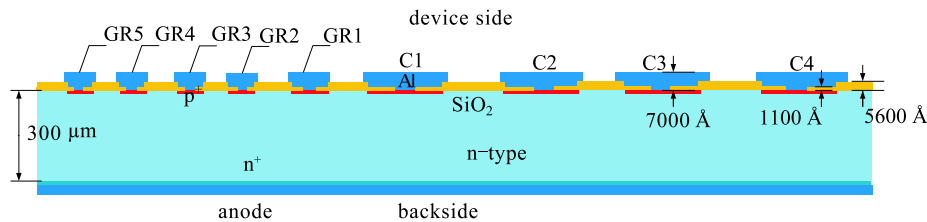

Fig. 1.   (color online) Cross-section of pixel sensor with five guard rings on a wafer of 300 μm thickness

Figure 2 shows the basic SPS fabrication process in our experiments. The various fabricated SPS arrays and the test device structure are shown in Fig. 3. The fabrication flow is as follows. On the device side of the high-resistivity Si substrate, a layer of original 5600 Å silicon dioxide is grown by wet oxide. This step needs to be controlled carefully to get a good quality oxide at the Si-SiO$_2$ interface whereas the bulk oxide charge created by long-time oxidation leads to some degradation beneath diode leakage characteristics. The first lithography was carried out to generate the p$^+$ pattern, followed by the remove of the initial oxide. Then, the gate-oxide was grown on the p$^+$ area. Next, a boron implantation through silicon dioxide was used to form the p$^+$ doping regions. Wet etching was then performed to remove

the gate oxide layer which covered the metal contact positions. On the entrance window side of the Si wafer, a phosphorus implantation was used to form the ohmic contact side, following by an annealing step for doping activations. In the following steps, the contact windows are formed with another lithography and etching process. Both on the device side and entrance side, thick aluminum layers were deposited, and the film on the device side was then patterned into the electrodes. The entrance window side is radiation hard due to the lack of silicon dioxide between the heavy doping and the aluminum layer. The process followed requires only three masks and no photolithographic steps are applied on the backside.
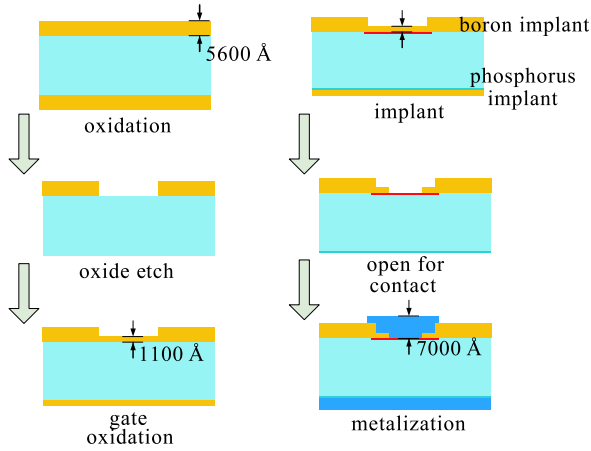
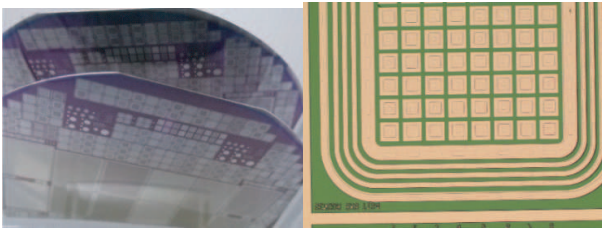Fig. 2.   (color online) Fabrication flow of SPS in our experiments.

Fig. 3.   (color online) Image of fabricated SPSs on Si wafers.

3   Optimizations of pixel sensors

The implemented device type of our SPS is a PIN diode located in a large array. The pixel sensor is designed as a single side planar structure with PIN diodes having p$^+$-implantations in an n-type substrate. The pixels are the signal collecting electrode (cathode) applied with ground potential, and the backside (anode) is applied with positive full depletion voltage as sketched in Fig. 1. This leads to the electrons drifting to the anodes and the holes drifting to the cathodes. We performed many processes and device emulations on TCAD tools for the optimization of some critical SPS parameters. First, the junction depth during ion implantations needs to be adjusted because this parameter determines the dead layer in X-ray detection, as the junction area cannot act as an absorption region but as the collected charge region. The guard rings area was also simulated to understand the potential distribution and to avoid breakdown for the case of high voltage applied to the sensor. The full depletion voltage is one of the important parameters for the pixel sensor working above the full depletion voltage for maximum quantum efficiency.

3.1   Junction depth with implant energy

The junction region forms a dead region for X-ray detection. In order to minimize the dead region, shal-

low implant and junction should be used in pixel sensors. To determine the junction depth, we simulated the boron implantation process using TCAD. Fig. 4 shows the boron doping profiles after doping annealing with different implantation energies and the same implant dose. The boron implantations on the device side form the p$^+$-n junction with n-type substrate. In consideration of the junction depth requirement and technology limit, we choose an implant energy of 35 keV, which makes the junction depth about 1μm. The backside implant of phosphorus was to form the ohmic contact with the aluminum electrode. In the simulation process, the gate oxide was also used to serve as the implant stop layer to decrease the substrate damage.
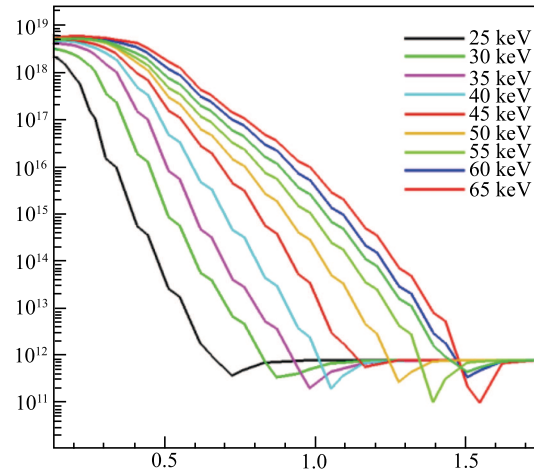

Fig. 4.   (color online) Simulated doping profiles for p$^+$ junctions by boron implantation with different implant energies and the same dose (6×10^{14}/cm^3)

3.2   Design of the guard ring area

The multi-guard ring structure is designed to form a gradual voltage drop between the sensitive region on ground potential and the cutting edge on backside potential [7–9]. This kind of structure is to reduce the dark current in the active region by decoupling the current generated outside the active region, and prevents the space charge region from reaching the cutting damage area. It also eliminates the high field region that causes avalanche breakdown. The guard rings are applied with ground potential or serve as floating rings and are self-biased via the punch-through mechanism. The number of guard rings and the width of the gaps are determined by the maximum applied voltage and the thickness of the sensor. By optimizing the number of guard rings and the gap distance, the dead region is minimized. Figure 5 shows the potential of the pixel sensor with five floating guard rings and the anode biased at 100 V. The potential drops slowly from the left guard ring to the pixel area.
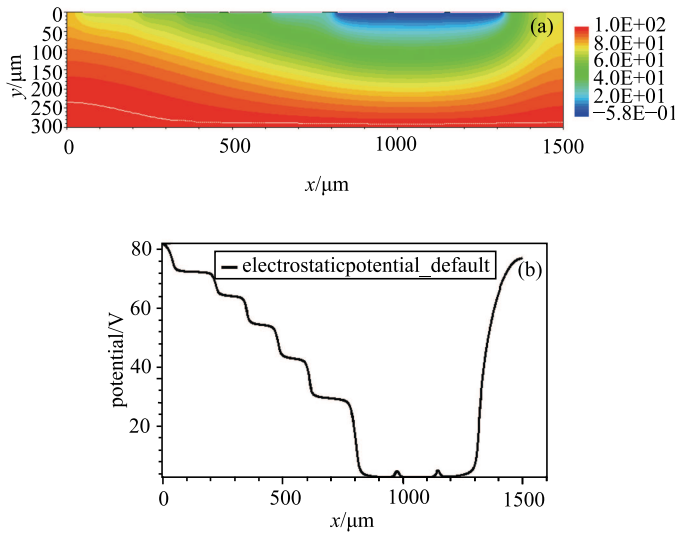
Fig. 5.   (color online)(a) potential distribution of pixel sensor with floating guard rings and the backside applied with 100 V and the device side with 0 V; (b) potential distribution along x direction while $y = 20$ μm

3.3   Heavy ion pulse response with different bias voltages

The pixel detector is used to detect single beam synchrotron X-ray irradiation, and X-ray photons may produce electron-hole pairs once the photons are absorbed in the silicon body of detector. For X-ray irradiation with an ultra-short wave length, the simulation of X-ray response becomes difficult for TCAD. Usually, TCAD can only simulate responses to long wavelength photons such as visible light and infrared light. However, TCAD provides radiation models for simulation of injected electron-hole pairs. When high-energy particles penetrate a semiconductor device, they deposit their energy by the generation of electron-hole pairs, just like the X-ray photons. These charges can move along the electric field lines and induce current, and are then collected by the electrode at the end. We simulate the heavy ion response of the silicon device, and the induced current shows the process of charge collection. These simulations help the designs of the silicon device and the ASIC readout electronics. Figure 6 (a) shows the drifting of
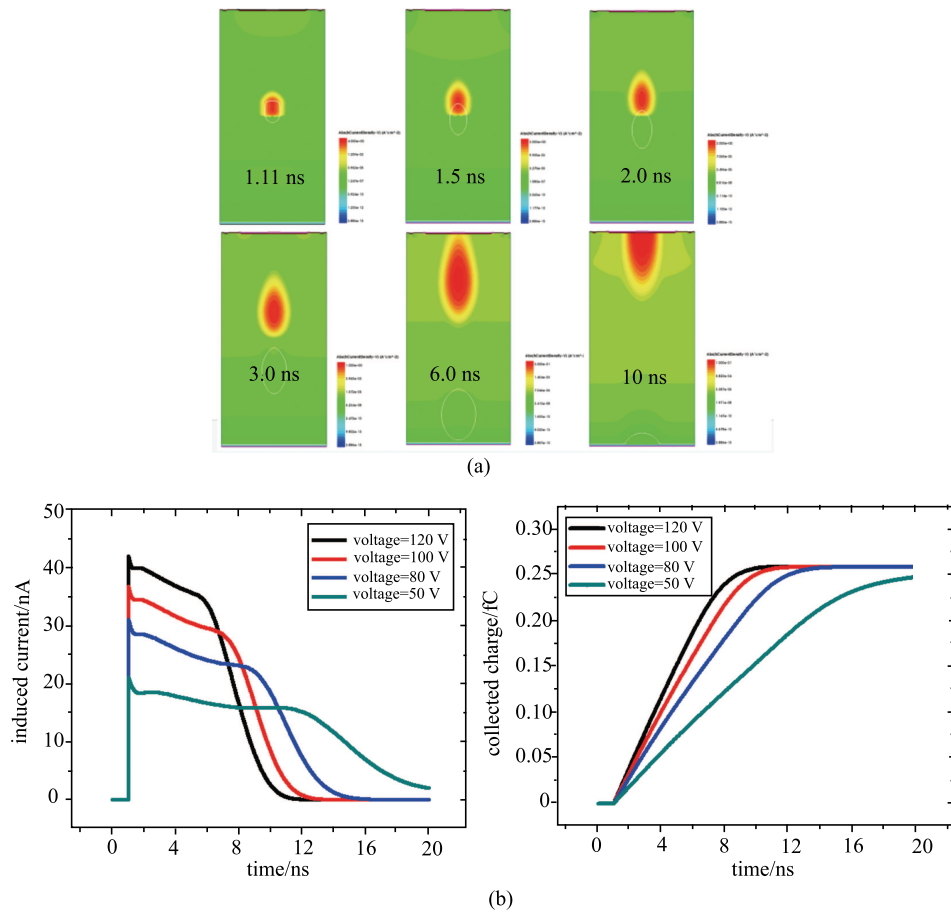

(a)

(b)

Fig. 6.   (Color online) (a) Drifting of generated current by induced holes from the initial position to the electrode at different time points, (b) collected charges at different bias voltage over time

hole current and the 2D mapping of generated current density at different time points. It clearly explains the collection process of electron-hole pairs during SPS irradiation. The generated charge-cloud spreads when it moves along the electrical field and this expansion causes the effect of charge sharing, especially in small pixels. In Fig. 6(b), the total induced current and charge vary with time. The total current decreases to zero at about 12 ns with voltage equal to 100 V, therefore, the charge signal is fully collected within 12 ns. The bigger the bias voltage, the faster the charge is collected, but the bias voltage should not exceed the breakdown voltage.

4   Electrical characteristics of SPS and response to synchrotron radiation

After the SPSs were fabricated, the electrical properties, including full depletion capacitance of pixels and the total leakage current of different structures of pixels, were measured. Also, the SPS sensors were bonded to an ASIC circuit to test the response to X-ray radiation at the Beijing Synchrotron Radiation Facility (BSRF). The characteristics of the SPSs for SRD were carefully investigated.

4.1   C-V characteristics and full depletion voltage

In order to collect the full charge in the detector, the SPS has to be fully depleted by applying $V_{\mathrm{bias}} > V_{\mathrm{FD}}$ in reverse bias conditions. The bulk capacitance per unit area is determined by the depth of the depletion layer (w),

$$C_{\mathrm{bulk}} = \frac{\varepsilon_{\mathrm{Si}}}{w} = \sqrt{\frac{\varepsilon_{\mathrm{Si}}}{2\mu\rho V_{\mathrm{bias}}}}, \qquad (1)$$

where μ is the mobility and ρ is the resistivity of the silicon substrate. D is the thickness of the substrate. When the bulk is fully depleted, w should be equal to D and Eq. (1) resolves to

$$V_{\mathrm{FD}} = \frac{D^2}{2\varepsilon_{\mathrm{Si}}\rho\mu}. \qquad (2)$$

After depleting the whole silicon substrate, the capacitance C_{bulk} becomes constant. Figure 7 shows the measured capacitance as a function of the reverse bias voltage. The results show good agreement between the fabricated sensors and simulation results for full depletion voltage below 50 V (right: measured results, left: simulation with two-dimension scale results).

4.2   I-V measurements and dark current

The dark current is the major parameter used to characterize a SPS. The dark leakage current and total pixel capacitance, including contact capacitance and bulk capacitance, are the major noise source of the readout system, and should be kept as low as possible. Usually, the bulk capacitance is constant when $V_{\mathrm{bias}} > V_{\mathrm{FD}}(< 50 \text{ V})$, which stays constant, and the contact capacitance may be decreased by integration with indium bump bonding technology. The leakage current is proportional to the depletion layer thickness d of the sensor, which is proportional to $V_{\mathrm{bias}}^{1/2}$, so it stays constant after reaching V_{FD} before the sensor approaches breakdown. We tested the single pixel leakage current of T1S1–T1S4, T2S2–T2S4, T3S3 and T4S1 structures, and the total leakage current of 8×8 pixels with the T1S1 structure. The test results are shown in Fig. 8 and demonstrate a typical leakage current at the 0.1 nA level for a single pixel with general structure, 0.5 nA level for 8×8 pixels without grounded guard rings, and 0.05 nA level for 8×8 pixels with grounded guard rings while V_{bias}=50 V. The standard pixel size is 200 μm×200 μm with 20 μm gap, therefore, the total area of 8×8 pixels is about 2.56 mm². From these test results, it is deduced that major electrical characteristics of the developed SPS are all excellent with a dark current of 2 nA/cm², full depletion voltage below 50 V and breakdown voltage greater than 150 V.
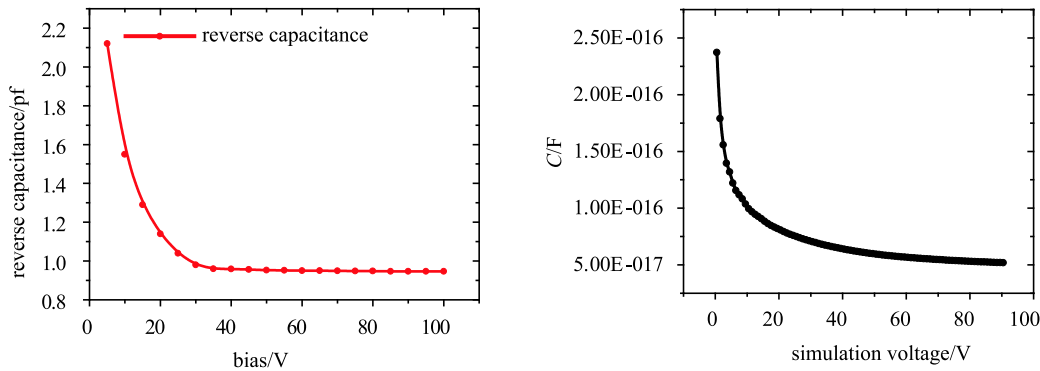

Fig. 7.   Measured reverse capacitance as a function of bias in fabricated SPS, where the reverse capacitance reaches a minimum value when the bias voltage reaches the value of the full depletion voltage.
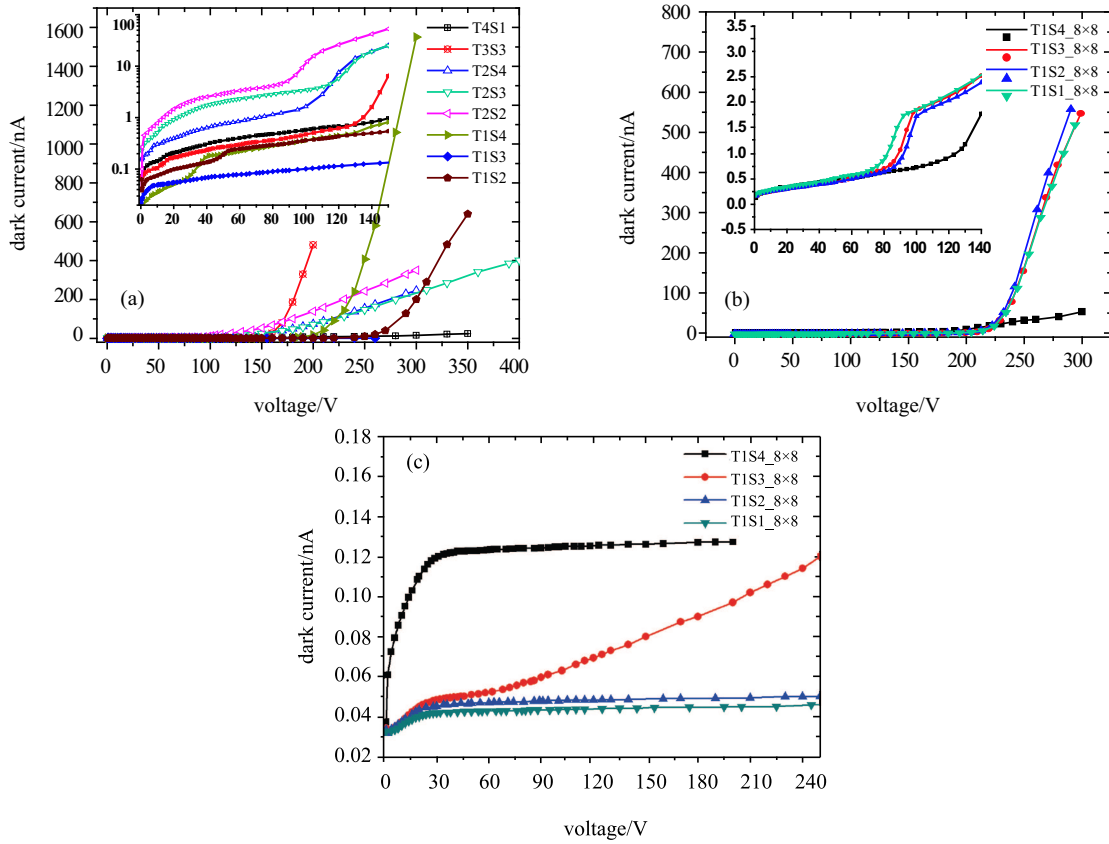
Fig. 8.   (color online) Measured dark currents plotted as functions of bias voltage for different SPSs: (a) Single pixel leakage current of T1, T2, T3, T4 structureswithout grounded guard rings, and total 8×8 pixels leakage current of T1 structure (b) without and (c) with grounded guard rings.

The leakage current distributions across the fabricated silicon wafer were different because of some process variations and the edge effect for outside sensors. The leakage currents of outer pixels are generally larger than those of inner pixels. Figure 9 shows the distribution of 8×8 pixels leakage current, with the leakage current of inner pixels obviously smaller than that of the outer pixels.
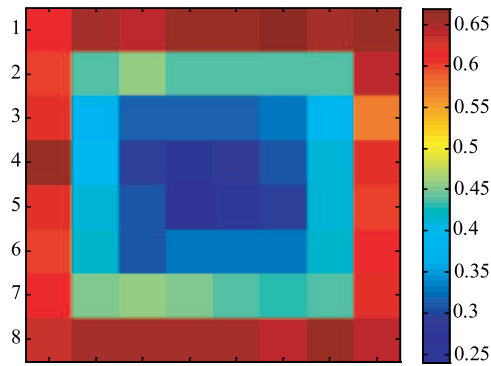

Fig. 9.   (color online)Leakage current (unit/nA) distribution of 8×8 pixels, where the dark current of outer pixels is larger than that of inner pixels.

4.3   Synchrotron radiation test

Figure 10(a) shows the fabricated SPSs bonded to the ASIC circuit by wires. For rapid testing, we connected four pixels to the ASIC readout circuit and tested the X-ray response. Figure 10(a) shows the technical details of the pixels and the inner guard ring bonded to the circuit. The synchrotron beam line is generated from BSRF beam line 1W2B for SPS testing and the X-ray energy varies from 8 keV to 18 keV. Figure 10(b) shows the experimental facility for our SPS test. The collimation hole is used for the X-ray collimation and the X-ray intensity is easily tuned by rotating the dial.

The integrated ASIC includes a charge sensitive preamplifier, shaping circuit, and threshold discriminating circuit. Figure 11 shows the measured signals from 8 keV X-ray photons irradiating the SPSs. The upper signal curve (red line) is the output signal of the charge sensitive preamplifier. The ASIC automatically counts while the signal amplitude is larger than the threshold value for discrimination, which is set via an Equivalent Generator, and the signal curve (green line) is also shown in Fig. 11. The measured signal amplitude varies with different X-ray photon energies. For a fixed X-ray
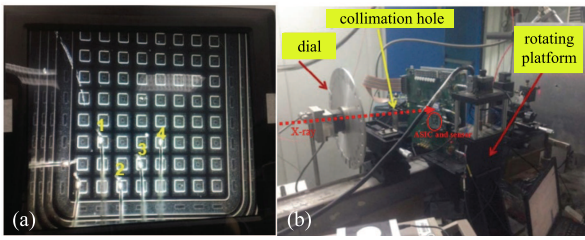
Fig. 10.   (color online)(a) Photograph of 8×8 pixel sensor with four pixels bonding to ASIC by wires for irradiation test, (b) the synchrotron X-ray test facility, where the X-ray beam directly irradiates the device side of the sensor.

energy, the signal from the shaping circuit should be constant. When the threshold value is larger than the test signal, the counting is zero, otherwise the counting is the number of X-ray photons. Figure 12 shows the counting performance of the fabricated SPS at different X-ray energies. Four fabricated pixels show the same trend
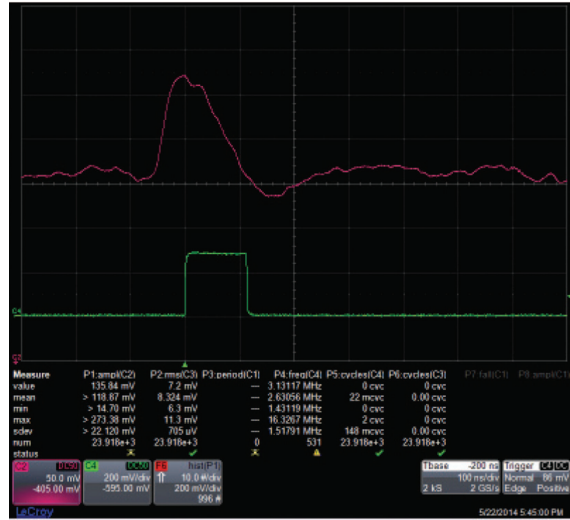

Fig. 11.   (color online) Measured analog output signal of ASIC (red line) and discriminator output (green line) for SPS under X-ray irradiation.
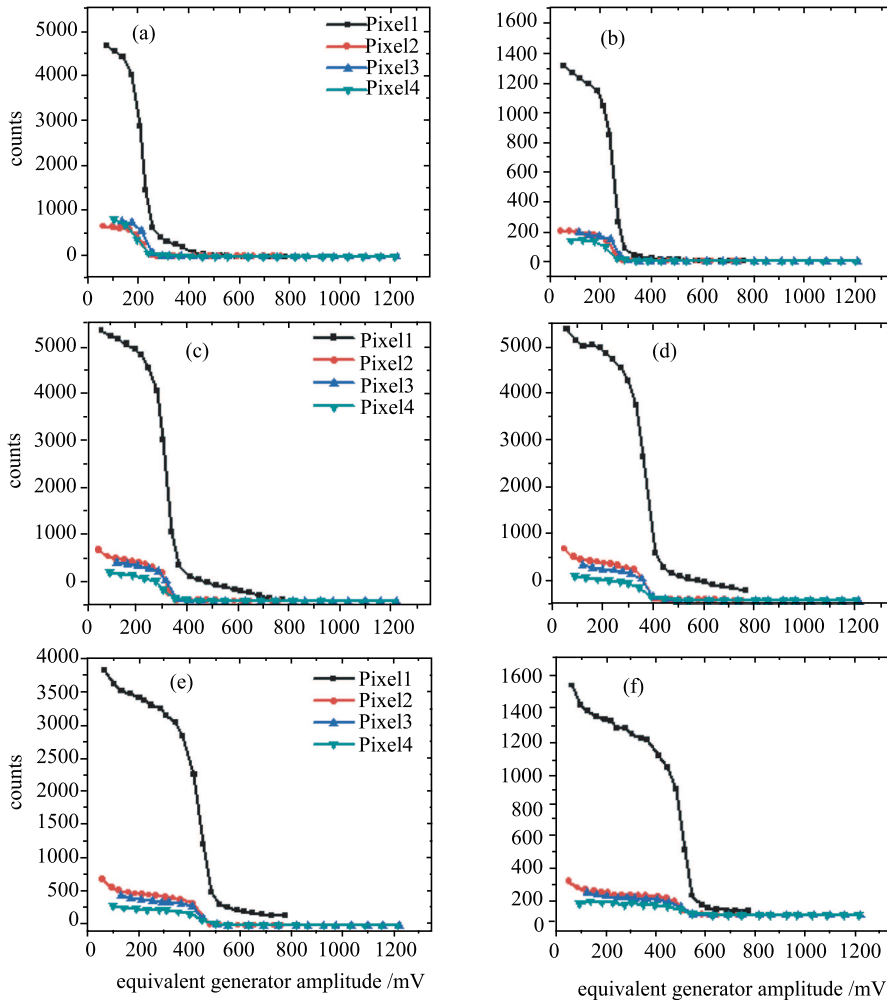

Fig. 12.   (color online) Measured counting performances for four pixels for different equivalent generator amplitudes while incident X-ray photo energies are(a) 8 keV, (b)10 keV, (c) 12 keV, (d) 14 keV, (e) 16 keV and (f) 18 keV.
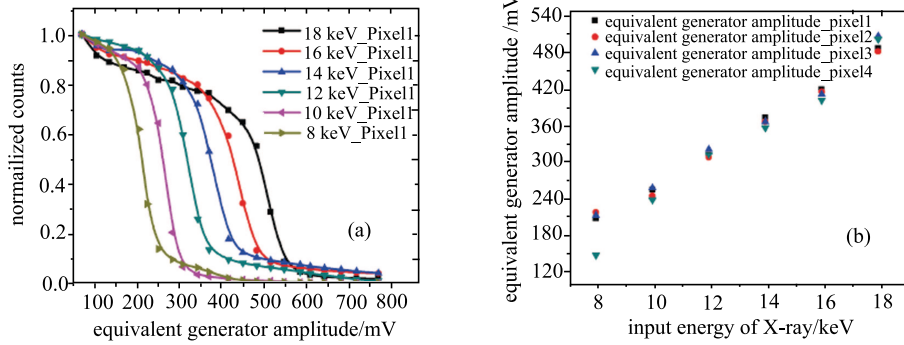
Fig. 13.   (color online) (a) Normalized count ability of pixel 1 at different photo energies, (b) linear relationship between the equivalent generator amplitude and the energy of the input X-ray.
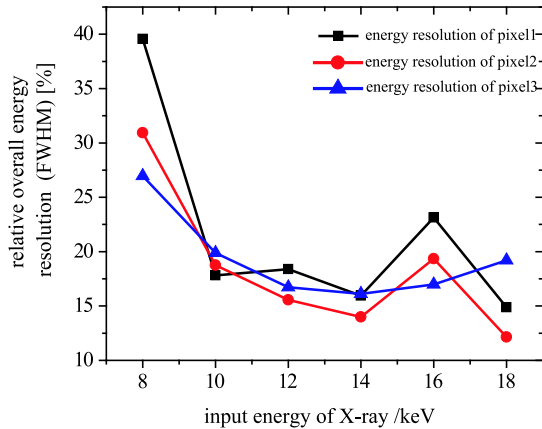

Fig. 14.   (color online) Extracted energy resolution of three pixels at different energies.

for the photon counting. The counted photon number of pixel 1 is the largest and became saturated, and the numbers counted by the other three pixels are very small due to the different distribution of the incident light spot. This indicates that the fabricated SPSs have strong photon counting ability and fast count rate for different X-rays. Figure 13(a) shows the radiation response of pixel 1 to different energies. The response S-lines are obviously distinguished from each other for different energies. In Fig. 13(b), the extracted equivalent generator amplitude from the falling-region of the response S-lines are linearly proportional to X-ray energy. This indicates that the linear response between the equivalent generator amplitude and the incident X-ray energy are properly established for precise SRD and confirms that the fabricated SPS demonstrates clear recognition of the energy changes during SRD.

The energy resolution of the fabricated SPS varies with input X-ray energy, as shown in Fig. 14. The differential of the S-lines in Fig. 13(a) is the energy spectrum of the SPS response. The energy resolution is defined by the formula of Energy Resolution=FWHM Energy, where FWHM is the full width at half maximum of the

response lines. From Fig. 14, it is concluded that the energy resolution increases as the photon energy increases. A better energy resolution is achieved for the fabricated SPS under higher energy SRD. On the other hand, the fabricated pixels in this manuscript were bonded to the ASIC circuit by wires, so the stray capacitance would be larger than if bonded via advanced flip-chip indium bump bonding. In future, the energy resolution of SPS may be further improved by flip-chip indium bump bonding.

5   Summary and outlook

In this paper, the design, fabrication and characterization of SPSs for a hybrid pixel single-photon-counting detector aiming at high performance SRD have been thoroughly studied. Using the theoretical principles of semiconductor devices and processes, the device structure and the SPS fabrication technology are optimized. Excellent electrical characteristics for the SPS, with dark current of 2 nA/cm², full depletion voltage < 50 V and breakdown voltage > 150 V, have been achieved. The response to X-ray irradiation has been tested with wire bonding to ASIC circuits. The results show that the fabricated SPSs have fast count rate, high energy resolution and good linearity to the photon energy of input X-rays. This means that the optimized SPS is promising for applications in high performance SRD systems. This is expected to be a strong technical contribution for the development of SRD in BAPS. The technology will be applied to the fabrication of 72×104 SPSs with pixel size of 150 μm for the integration of a real hybrid SRD system, which will be first used in biomacromolecule structure elucidation in BAPS. The reported SPS is expected to supply the basic sensing part for fast count rate and high energy resolution in the system. The response to synchrotron X-ray detection will be further improved with an improved package technology of indium bump bonding in the real SRD system.

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