Total dose radiation effects on SOI NMOS transistors with different layouts

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Abstract Partially-depleted Silicon-On-Insulator Negative Channel Metal Oxide Semiconductor (SOI NMOS) transistors with different layouts are fabricated on radiation hard Separation by IMplanted OXygen (SIMOX) substrate and tested using 10 keV X-ray radiation sources. The radiation performance is characterized by transistor threshold voltage shift and transistor leakage currents as a function of the total dose up to 2.0×10^6 rad(Si). The results show that the total dose radiation effects on NMOS devices are very sensitive to their layout structures.

Key words SIMOX, SOI, total dose radiation effect, MOS transistors

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1 Introduction

SOI technology is very promising for radiation-hard applications. The small charge-collection volume and p-n junction area of the SOI integrated circuits (ICs) have advantages of single event upset and high dose rate transient upset effects over bulk silicon ICs. However, unless radiation hardened, the total dose radiation effects will degrade the performance and reliability of SOI MOS transistors and ICs[1]. It is found that the radiation-induced positive charges are trapped not only in the buried oxide but also in the lateral oxide isolation regions (field oxide structures) which create a back-channel conduction path and edge leakage paths in the NMOS transistors.

We have recently reported that partially depleted SOI MOS transistors, fabricated in a standard 3 μm SOI CMOS (Complementary MOS) process, could achieve radiation hard performance by hardening the buried oxide and prevent back channel conduction in very harsh radiation environment[2—4]. We have been pursuing aggressively the development of radiation hard SOI CMOS device structures for designing radiation hard circuits to meet challenges in the near future space application.

In this work, NMOS transistors with different lay-out structures were fabricated by a standard 0.8 μm SOI CMOS process and subjected to total dose radiation analysis by X-ray irradiation experiments. The key radiation sensitive parameters such as the threshold voltage shift and the leakage currents as a function of total dose have been investigated and discussed. The roles of transistor layout structures and experiment conditions in the total dose radiation have also been addressed.

2 Experiment details

2.1 Devices

The NMOS transistors studied in this work were fabricated using the radiation hard SIMOX wafers with a buried oxide thickness of 375 nm and a top silicon thickness of 200 nm. The radiation hard wafers were formed through implanting silicon at a dose of 1×10^{15} cm^{-2} into the buried oxides and then annealed at 800℃ in N^2 ambience. These transistors were fabricated in a standard commercial 0.8 μm SOI CMOS process. The processing steps include isolation, well definition, gate oxidation, poly-silicon gate definition, lightly doped drain (LDD), source/drain implant, contact cut, and first metal. These NMOS transistors were designed with three different layout
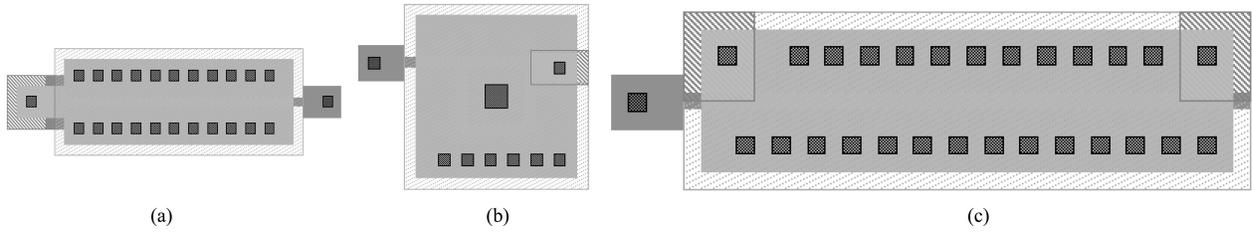
Fig. 1.   Schematic diagram of three different gate structures. (a) The single-stripe poly transistor; (b) The enclosed-gate transistor; (c) The body-tied-to-source (BTS) transistor.

structures: a standard single-stripe poly transistor, an enclosed-gate transistor and a body-tied-to-source (BTS) transistor, as shown in Fig. 1. Body ties were used in all the devices to suppress floating body effects. The channel lengths of all transistors were 0.8 µm and channel widths were 24 µm and a LOCal Oxidation of Silicon (LOCOS) oxide was used for transistor isolation.

2.2   Experiment

The 10 keV X-ray irradiations were performed on transistors at packaged part level (without lids) using an ARACOR Model 4100 Semiconductor X-ray Irradiator. The devices were irradiated with a total dose of about 2 Mrad(Si) at a rate of 30 krad(Si)/min. Bias to the parts was established just before each irradiation, and removed within 10—15 s after irradiation, and I-V measurements were taken with a computer controlled HP4156A parametric analyze. From some reported papers and our earlier work, the worst case irradiation conditions for NMOS transistors were the pass-gate irradiation bias [biased with 5 V on the drain and source, with all other terminals (gate, body and substrate) grounded][5—7]. Therefore, in this paper, we only compare and analyze the dada of different device structures under pass-gate bias.

3   Results and discussion

Figure 2(a, b) show the radiation responses of I-V characteristics of a back channel and a front channel 24/0.8 single-stripe poly NMOS transistor, respectively.

It can be seen from Fig. 2(a) that the current humps occur in the back channel I-V characteristic curves of the single-stripe poly NMOS transistor after irradiation. This is because the parasitic MOS devices are turned on by the total-dose-induced charge collected in the LOCOS region. These parasitic devices induce a high leakage current which has a direct impact on the I-V curves measured for the front-gate transistor, causing a high off-state current, as shown in Fig. 3(b).

The radiation responses of I-V characteristics of a

back channel and a front channel 24/0.8 enclosed-gate NMOS transistor are shown in Fig. 3(a) and Fig. 3(b), respectively.
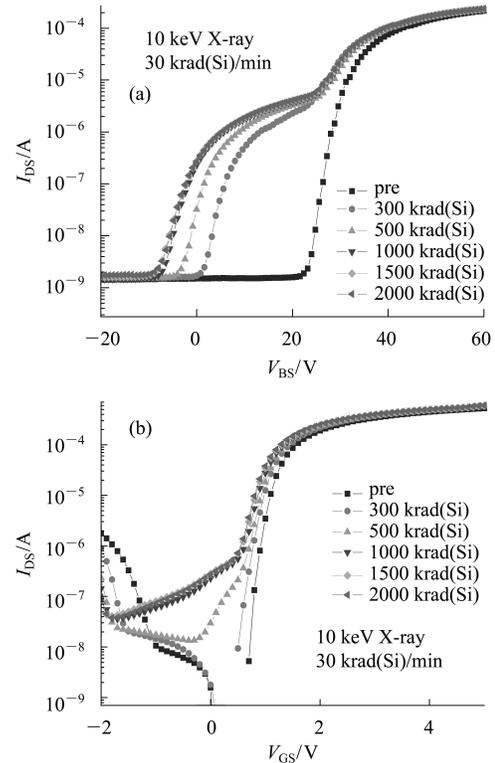

Fig. 2.   Back channel (a) and front channel (b) I-V curves of single-stripe poly NMOS transistor after different total dose irradiation under pass-gate bias.

Comparing the results of the devices with enclosed-gate and single-stripe poly layout structures, it can be seen that the leakage drain currents of the enclosed-gate transistor are much lower than the leakages of the single-stripe poly transistor under the worst-case bias conditions. Therefore, the enclosed-gate transistor can provide a great improvement in total-dose radiation tolerance than the single-stripe poly transistor. The main reason is that the enclosed-gate Field Effect Transistor (FET) has drain or source, but not both, on the two sides of the bird's beak region. Hence, even if there is a channel formed in that region, there is no potential across it to induce current flow[8].
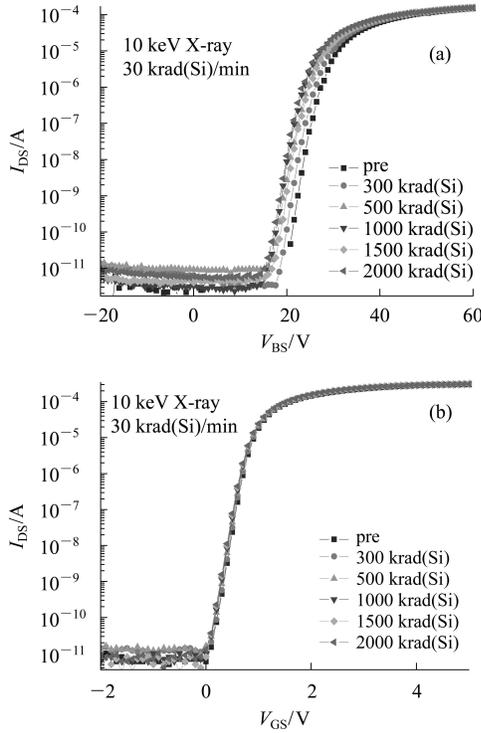
Fig. 3.   Back channel (a) and front channel (b) *I-V* curves of enclosed-gate NMOS transistor after different total dose irradiation under pass-gate bias.

The radiation induced threshold voltage shift of a 24/0.8 front channel enclosed-gate NMOS transistor is shown in Fig. 4(a). Little radiation induced front channel threshold voltage shift is observed (<0.2 V at 2×10^6 rad(Si)). For the 24/0.8 black channel enclosed-gate NMOSFET (as shown in Fig. 4(b)), the back channel threshold voltage shift is approximately -6 V and the final back channel threshold voltage at 2×10^6 rad(Si) is $>+20$ V.

The radiation responses of *I-V* characteristics of a back channel BTS NMOSFET under pass-gate radiation bias are shown in Fig. 5(a). Although a large voltage shift (13 V) is seen, the back channel threshold voltage is $= +25$ V at 2 Mrad(Si); that is, a very large margin still exists for the back channel NMOS transistor.

Figure 5(b) shows the radiation responses of *I-V* characteristics of a front channel BTS NMOSFET under pass-gate radiation bias. It can be seen that no current humps occur in the *I-V* characteristic curves, which indicate that the edge leakage path can be suppressed by creating narrow p-type BTS tabs in the source side of the device at the edges of the island[9]. Very small radiation induced front channel threshold voltage shift is observed (<0.2 V at 2×10^6 rad(Si)), implying that the Impact of back channel threshold voltage shift on the characteristics of front channel can be negligible, also.
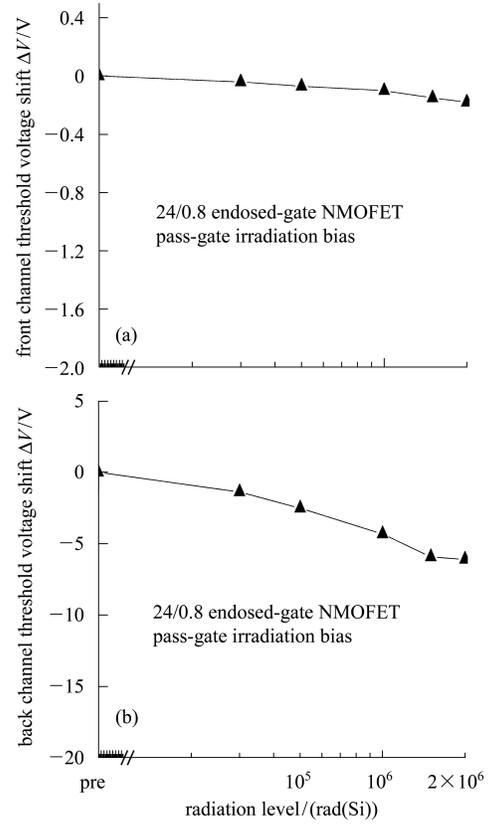

Fig. 4.   Radiation induced threshold voltage variation ΔV as a function of the total dose for a 24/0.8 front (a) and back (b) channel enclosed-gate NMOSFET.
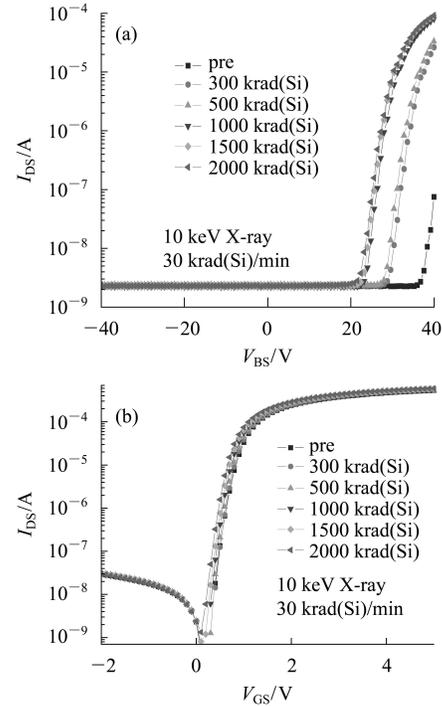

Fig. 5.   Back channel (a) and front channel (b) *I-V* curves of BTS NMOS transistor after different total dose irradiation under pass-gate bias.

Comparing Fig. 5(b) with Fig. 3(b), we find that for the BTS NMOSFET significant gate induced drain leakage (GIDL) current below zero V_{GS} exists, but the GIDL current is not visible for the enclosed-gate transistor. Since the GIDL current is caused by the band-to-band tunneling occurring in the deep-depletion layer in the gate-to-drain overlap region[10], the difference in response between the transistors may be caused by the differences in their layout structures, which affect the magnitude of oxide field in the gate-to-drain overlap region.

4 Conclusions

The total dose radiation effects on partially-depleted SOI NMOS transistors with single-stripe poly, enclosed-gate and body-tied-to-source layout structures have been studied by X-ray irradiation experiments. The test transistors were fabricated on radiation hard SIMOX substrate. The results show that the enclosed-gate and BTS layout structures can provide a great improvement in the total-dose radiation tolerance than the single-stripe poly shape as their structures can suppress the onset of any leakage current through a radiation induced lateral path under the bird's beak. In addition, the GIDL current was detected in BTS transistor, but not found in the enclosed-gate transistor. We attribute the difference in response between the transistors to the differences in their layout structures that affect the magnitude of oxide field in the gate-to-drain overlap region.

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